4:4 Cross-channel SuperSpeed Analog Switch IC CH9444

4:6 Cross-channel SuperSpeed USB Analog Switch IC CH9445

Datasheet

Version: V1.2

https://wch-ic.com

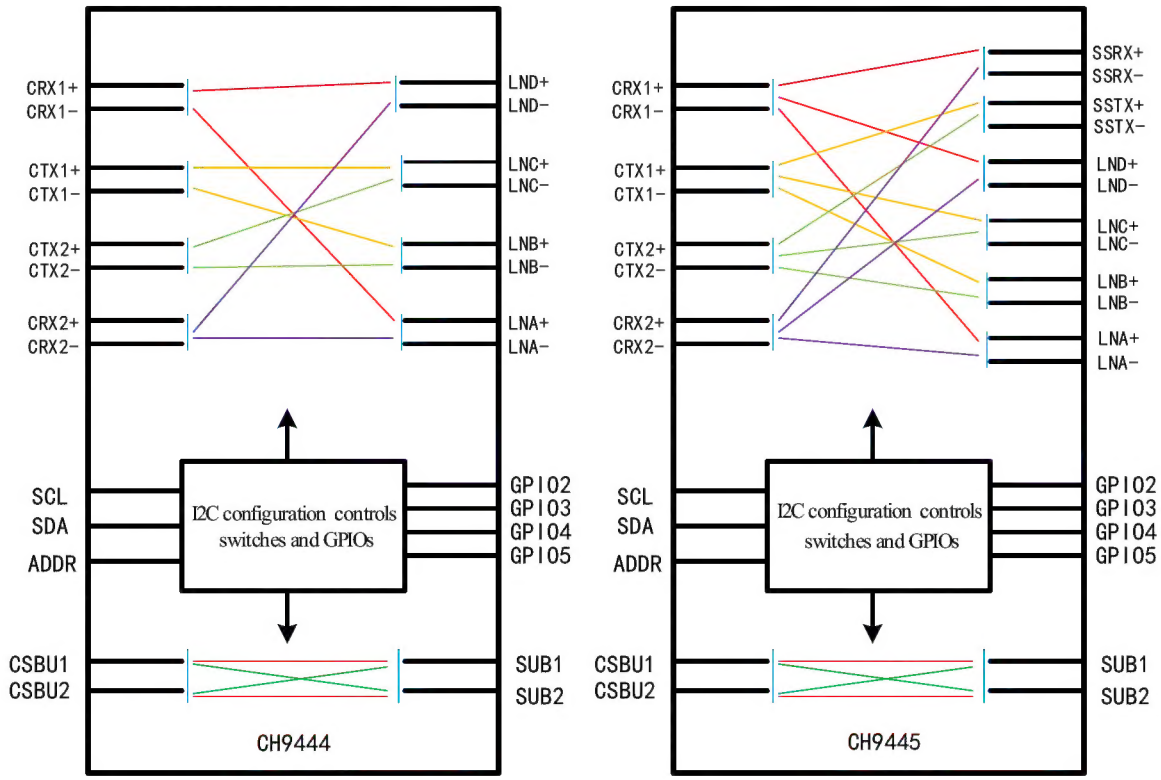
1. Overview

CH9444 and CH9445 are SuperSpeed differential signal bidirectional analog switch ICs, with high bandwidth and low ON resistance.

CH9444 can implement cross-channel switch of DP1.4 8Gbps, USB3.0, 480Mbps and other differential signals. CH9444 can be used in applications such as Type-C to 4 Lane DP for tablet PCs, laptop PCs and HUBs.

Compared with CH9444, CH9445 provides 2 more pairs of differential signal pins and added USB3.1 channel. CH9445 supports USB 10Gbps differential signal, and it can be used in applications such as Type-C to 2 Lane DP+USB3.

Internal block diagram for reference:

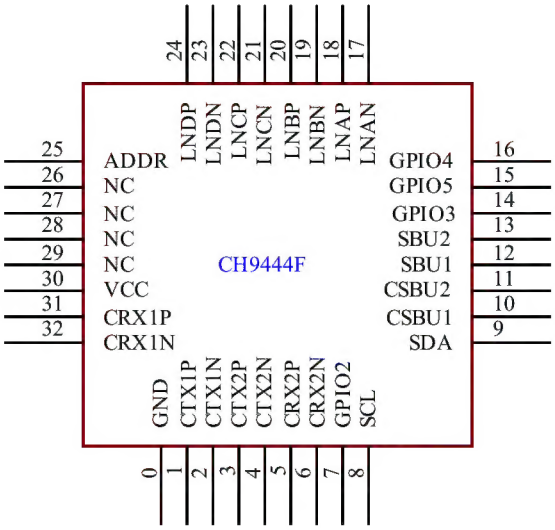


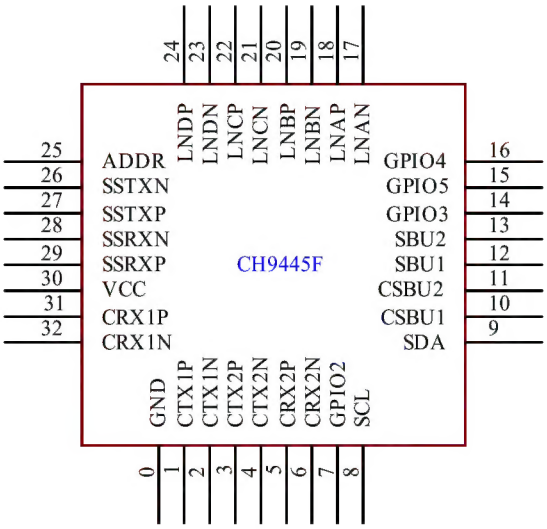
2. Features

- 4:4 or 4:6 cross-channel super-speed differential signal MUX switch.
- Support USB3.1 10Gbps signal.
- Support 8Gbps DP1.4 signal.
- Cross-channel Mux for CSBU and SBU pins.
- Control and configure MUX switching through I2C interface.
- 4 GPIO pins, support interrupt.

- Support low-power mode.
- Package: QFN32-4×4mm.

3. Package





Package	Body size	Lead pitch		Description	Part No.
QFN32-4*4	4*4mm	0.40mm	15.7mil	Quad Flat No-Lead Package	CH9444F
QFN32-4*4	4*4mm	0.40mm	15.7mil	Quad Flat No-Lead Package	CH9445F

Note: For QFN package, the EPAD is marked as 0# pin.

4. Pin Definitions

CH9444F pin No.	CH9445F pin No.	Pin Name	Pin Type	Description
30	30	VCC	Power	Positive power, rated 3.3V.
0	0	GND	Power	Ground
1, 2	1, 2	CTX1P, CTX1N	I/O	Analog switch port #0, can be connected to Type-C TX1 positive/negative port
3, 4	3, 4	CTX2P, CTX2N	I/O	Analog switch port #1, can be connected to Type-C TX2 positive/negative port
31, 32	31, 32	CRX1P, CRX1N	I/O	Analog switch port #2, can be connected to Type-C RX1 positive/negative port
5, 6	5, 6	CRX2P, CRX2N	I/O	Analog switch port #3, can be connected to Type-C RX2 positive/negative port
7, 14 15, 16	7, 14 15, 16	GPIO2, GPIO3 GPIO5, GPIO4	I/O	GPIO pins, 3-state bidirectional input and output
8	8	SCL	I	I2C clock pin input
9	9	SDA	I/O	I2C bidirectional data pin, open-drain output
10, 11	10, 11	CSBU1, CSBU2	I/O	Analog switch port #4/#5, can be connected to Type-C SBU1/SBU2 port
12, 13	12, 13	SBU1, SBU2	I/O	Analog switch port #6/#7, can be selected to be on with CSBU1/CSBU2
17, 18	17, 18	LNAN, LNAP	I/O	Analog switch port #8, can be connected to DP A negative/positive port
19, 20	19, 20	LNBN, LNBP	I/O	Analog switch port #9, can be connected to DP B negative/positive port
21, 22	21, 22	LNCN, LNCP	I/O	Analog switch port #10, can be connected to DP C negative/positive port
23, 24	23, 24	LNDN, LNDP	I/O	Analog switch port #11, can be connected to DP D negative/positive port
25	25	ADDR	I/O	Input: I2C device address. Output: GPIO interrupt signal
	26, 27	SSTXN, SSTXP	I/O	Analog switch port #12, super-speed channel TX negative/positive port
	28, 29	SSRXN, SSRXP	I/O	Analog switch port #13, super-speed channel RX negative/positive port
26~29		NC.		Not connected.

5. Functional Description

CH9444 is a super-speed bidirectional 4×4 and low-speed 2×2 cross-point analog switch IC, supporting DP1.4 up to 8Gbps, USB3.0 and USB2.0. CH9444 can not only configure MUX switching for 2ch/4ch DP lane but also provide cross-point MUX for low-speed side band communication.

CH9445 is a super-speed bidirectional 4×6 and low-speed 2×2 cross-point analog switch IC. Compared with CH9444, CH9445 adds USB3.1 signal channel, supports USB3.1 Gen2 up to 10Gbps, and can configure MUX switching for USB3.0/3.1.

Registers of CH9444 and CH9445 are divided into system registers and GPIO control registers. The system registers are mainly used for switch control. The GPIO control registers can be used to control 4 GPIOs independently.

5.1. System Register

Table-1 System registers

Name	Address	Description	Reset value
CVR	0x08	Chip version register	0x00
MUX_PDR	0x10	MUX power down register	0x00
MUX_CTLR	0x11	MUX control register	0x00
SYS_CTLR0	0x30	System control register 0	0x00
SYS_CTLR1	0x31	System control register 1	0x00
SYS_CTLR2	0x32	System control register 2	0x00

Chip Version Register (CVR)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:0]	CHIP_V	RO	Chip version number: 0x00 by default.	00h

MUX Power Down Register (MUX_PDR)

Bit	Name	Access	Description	Reset value
[7:1]	-	RO	Reserved	00h
[0]	MUXPD	RW	Mux power down: 0: Power on. Switches can be controlled. 1: Power down. All switches are off and cannot be controlled.	0b

MUX Control Register (MUX_CTLR)

Bit	Name	Access	Description	Reset value
[7:5]	-	RO	Reserved	00h
[4]	POL	RW	MUX control select register 2: 0: L. 1: H. Note: See Table-2 for the result related to POL, CT1 and CT0.	0b
[3:2]	CT1	RW	MUX control select register 1: 00: L. 01: M.	00b

			10: Reserved. 11: H. Note: See Table-2 for the result related to POL, CT1 and CT0.	
[1:0]	CT0	RW	MUX control select register 0: 00: L. 01: M. 10: Reserved. 11: H. Note: See Table-2 for the result related to POL, CT1 and CT0.	00b

System Control Register 0 (SYS_CTLR0)

Bit	Name	Access	Description	Reset value
[7:3]	-	RO	Reserved	00h
[2]	ADR_INT_EN	RW	ADDR interrupt enable: 0: ADDR is the input state, as the device address selection and configuration. 1: ADDR will output GPIO interrupt signal. Note: ADDR is latched when this bit is set, as the I2C device address selection. The latch cannot be released until this bit is cleared. Please confirm that the ADDR pin is not directly shorted to VCC or GND before this bit is set. If it also needs to be used as an address input, it is recommended to select a pull-up resistor or a pull-down resistor of dozens of KΩ or hundreds of KΩ.	0b
[1:0]	SEL_SW[1:0]	RW	Low-speed MUX switch: 01: Cross conduction between CSBU and SBU. 10: Direct conduction between CSBU and SBU. Others: Switch off.	00b

System Control Register 1 (SYS_CTLR1)

Bit	Name	Access	Description	Reset value
[7:4]	SEL_B[3]	RW	Switch control 0: Off. 1: On.	0h
	SEL_B[2]		Switch control 0: Off. 1: On.	
	SEL_B[1]		Switch control 0: Off. 1: On.	
	SEL_B[0]		Switch control 0: Off. 1: On.	
[3:0]	SEL_A[3]	RW	Switch control 0: Off. 1: On.	0h
	SEL_A[2]		Switch control 0: Off. 1: On.	
	SEL_A[1]		Switch control 0: Off. 1: On.	
	SEL_A[0]		Switch control 0: Off. 1: On.	

Note: SEL_B[Y](Y=0, 1, 2, 3) can be used to control states of SSRXN, SSRXP, LNBP and LNBN. For details, see Section 5.2 internal switch diagram.

System Control Register 2 (SYS_CTLR2)

Bit	Name	Access	Description	Reset value
[7:4]	SEL_D[3]	RW	Switch control 0: Off. 1: On.	0h
	SEL_D[2]		Switch control 0: Off. 1: On.	
	SEL_D[1]		Switch control 0: Off. 1: On.	
	SEL_D[0]		Switch control 0: Off. 1: On.	
[3:0]	SEL_C[3]	RW	Switch control 0: Off. 1: On.	0h
	SEL_C[2]		Switch control 0: Off. 1: On.	
	SEL_C[1]		Switch control 0: Off. 1: On.	
	SEL_C[0]		Switch control 0: Off. 1: On.	

Note 1: SEL_D[Y](Y=0, 1, 2, 3) can be used to control states of SSTXN, SSTXP, LNDP and LNDN.
For details, see Section 5.2 internal switch diagram.

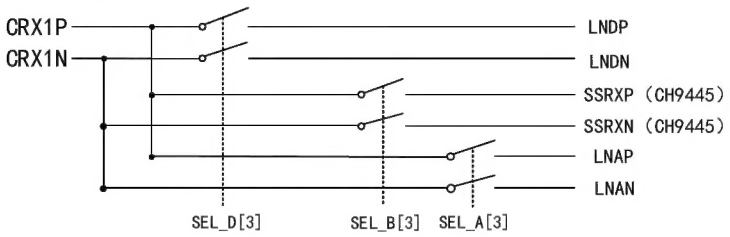
Note 2: The operations on SYS_CTLR0 take effect immediately. When performing write operation on SYS_CTLR1, the written value is not updated to the register in time, but is temporarily stored in the backup register, and then the values written to SYS_CTLR1 and SYS_CTLR2 are loaded into the registers at the end of the write operation on SYS_CTLR2 to control the switches and make sure all switches work simultaneously. So all switches work at the end of the write operation on SYS_CTLR2.

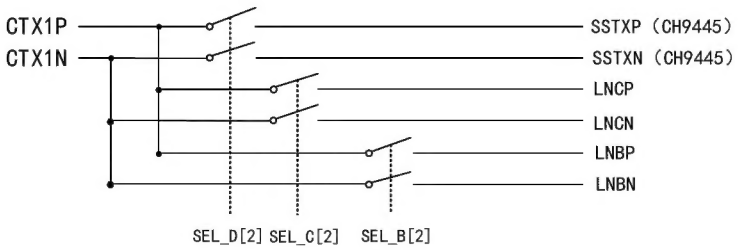
Table-2 MUX configuration table

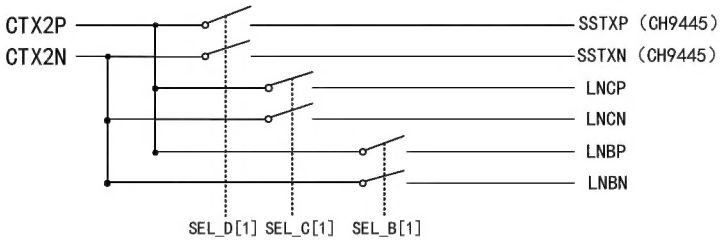
	ALL OFF	USB3.1/ USB3.1 flip		4 Ln DP/ 4 Ln DP flip		USB3.1LnA LnB/ USB3.1LnALnB flip		USB3.1 LnC LnD/ USB3.1LnC LnD flip		USB3.1 LnA LnC/ USB3.1LnA LnC flip	
[POL/CT1/CT0]	[X/X/L]	[L/M/H]	[H/M/H]	[L/H/H]	[H/H/H]	[L/L/H]	[H/L/H]	[L/L/M]	[H/L/M]	[L/M/M]	[H/M/M]
SSRX	X	CRX1	CRX2	X	X	CRX1	CRX2	CRX1	CRX2	CRX1	CRX2
SSTX	X	CTX1	CTX2	X	X	CTX1	CTX2	CTX1	CTX2	CTX1	CTX2
LNA	X	X	X	CRX2	CRX1	CRX2	CRX1	X	X	CRX2	CRX1
LNB	X	X	X	CTX2	CTX1	CTX2	CTX1	X	X	X	X
LNC	X	X	X	CTX1	CTX2	X	X	CTX2	CTX1	CTX2	CTX1
LND	X	X	X	CRX1	CRX2	X	X	CRX2	CRX1	X	X
SBU1	X	CSBU1	CSBU2	CSBU1	CSBU2	CSBU1	CSBU2	CSBU1	CSBU2	CSBU1	CSBU2
SBU2	X	CSBU2	CSBU1	CSBU2	CSBU1	CSBU2	CSBU1	CSBU2	CSBU1	CSBU2	CSBU1

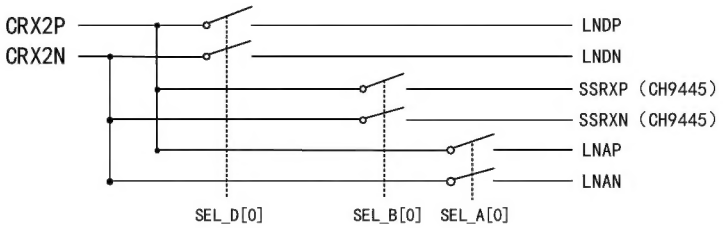
Note: CH9444 has no SSRX or SSTX.

5.2. Internal Switch Diagram

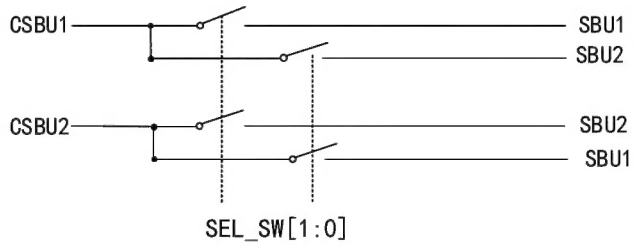








- SEL_X[Y]=1, switch on. SEL_X[Y]=0, switch off. (X=D, C, B, A. Y=3, 2, 1, 0).



- SEL_SW[1:0]=00 or 11, 4 switches all off.
- SEL_SW[1:0]=01, right side switches on (cross). SEL_SW[1:0]=10, left side switches on (pass through).

5.3. GPIO Control Register

The general-purpose I/O is composed of independent I/O pins controlled by registers. GPIO supports interrupt function. If the value of GP2~GP5 changes, an interrupt signal will be generated, and this signal can be edge triggered (rising/falling) or level triggered (high/low).

Table-3 GPIO registers

Name	Address	Description	Reset value
GPIO_DIR	0x20	GPIO direction register	0x00
GPIO_PIN	0x21	GPIO input value register	0xXX
GPIO_OUT	0x22	GPIO output value register	0x00
GPIO_IMR	0x23	GPIO interrupt trigger mode register	0x00

GPIO_TLR	0x24	GPIO interrupt trigger level register	0x00
GPIO_TER	0x25	GPIO interrupt trigger edge register	0x00
GPI0_ISR	0x26	GPIO interrupt status register	0x00
GPIO_INTENR	0x27	GPIO interrupt enable register	0x3C
GPIO_IAENR	0x28	GPIO interrupt all enable register	0x01
GPIO_PUDR	0x29	GPIO pull-up/pull-down register	0x00
GPIO_PUDER	0x2A	GPIO pull-up/pull-down disable register	0x00

GPIO Direction Register (GPIO_DIR)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_DIR	RW	GPIO direction select: 0: Input. 1: Output.	0h
[1:0]	-	RO	Reserved	00b

GPIO Input Value Register (GPIO_PIN)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_PIN	RO	GPIO input value select: 0: Input low level. 1: Input high level.	0Xh
[1:0]	-	RO	Reserved	00b

GPIO Output Value Register (GPIO_OUT)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_OUT	RW	GPIO output value select: 0: Output low level. 1: Output high level.	0h
[1:0]	-	RO	Reserved	00b

GPIO Interrupt Mode Register (GPIO_IMR)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_IMR	RW	GPIO interrupt trigger mode setting: 0: Level trigger. 1: Edge trigger.	0h
[1:0]	-	RO	Reserved	00b

GPIO Trigger Level Register (GPIO_TLR)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_TLR	RW	GPIO interrupt trigger level setting: 0: Low. 1: High.	0h
[1:0]	-	RO	Reserved	00b

GPIO Trigger Edge Register (GPIO_TER)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_TER	RW	GPIO interrupt trigger edge setting: 0: Falling. 1: Rising.	0h
[1:0]	-	RO	Reserved	00b

GPIO Interrupt Status Register (GPI0_ISR)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_ISR	RW	GPIO interrupt status bit. Write 0 to reset. 0: No interrupt. 1: Interrupt.	0h
[1:0]	-	RO	Reserved	00b

GPIO Interrupt Enable Register (GPIO_INTENR)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_INTENR	RW	GPIO interrupt enable: 0: Corresponding GPIO interrupt enabled. 1: Corresponding GPIO interrupt disabled.	0Fh
[1:0]	-	RO	Reserved	00b

GPIO Interrupt All Enable Register (GPIO_IAENR)

Bit	Name	Access	Description	Reset value
[7:1]	-	RO	Reserved	00h
[0]	GP_IAENR	RW	GPIO interrupt all enable: 0: Whether an interrupt is enabled or not depends on GPIO_INTENR. 1: All interrupts disabled.	1b

GPIO Pull-up/pull-down Register (GPIO_PUDR)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_PUDR	RW	GPIO pull-up/pull-down setting: 0: Pull down. 1: Pull up.	0h
[1:0]	-	RO	Reserved	00b

GPIO Pull-up/pull-down Disable Register (GPIO_PUDER)

Bit	Name	Access	Description	Reset value
[7:6]	-	RO	Reserved	00b
[5:2]	GP_PUDER	RW	GPIO pull-up/pull-down disable: 0: Pull-up or pull-down depends on GPIO_PUDR. 1: Pull-up/pull-down disabled.	0h

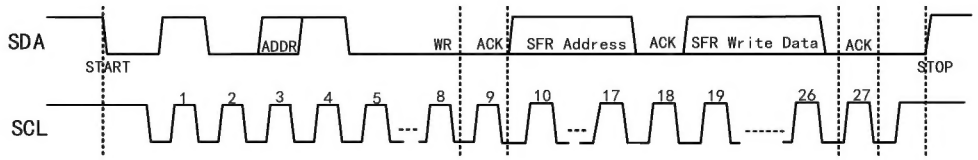
[1:0]	-	RO	Reserved	00b

5.4. Register Operation Description

Registers of CH9444 and CH9445 are accessed through I2C interface. The 7-bit device address depends on the level input by ADDR pin. The device address is 0x58 when the ADDR pin inputs high. While the device address is 0x48 when the ADDR pin inputs low.

ADDR Pin	I2C device address							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
L	1	0	0	1	0	0	0	0/1(W/R)
H	1	0	1	1	0	0	0	0/1(W/R)

5.4.1. Write Operation on the Register



Register write timings

As shown in the figure above, the procedure of the write operation on CH9444 and CH9445 is as follows:

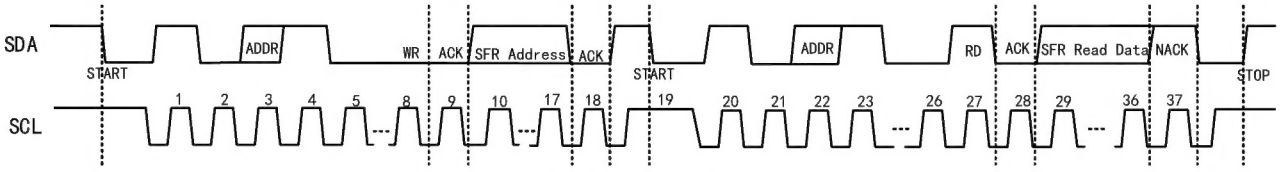
(1) I2C host generates a Start bit, transmits device address and writes control signal simultaneously, then waits for CH9444/CH9445 ACK.

(2) I2C host transmits the address of the write operation register, and waits for CH9444/CH9445 ACK.

(3) I2C host transmits the write data in bytes, and waits for CH9444/CH9445 ACK.

(4) I2C host generates a STOP bit after it gets ACK, ending the write operation.

5.4.2. Read Operation on the Register



Register read timings

As shown in the figure above, the procedure of the read operation on CH9444 and CH9445 is as follows:

(1) I2C host generates a Start bit, transmits device address and writes control signal simultaneously, then waits for CH9444/CH9445 ACK.

(2) I2C host transmits the address of the read operation register, and waits for CH9444/CH9445 ACK.

(3) I2C host generates a Start bit again, transmits device address and reads control signal simultaneously, then waits for CH9444/CH9445 ACK.

(4) I2C host gets the read data in bytes.

(5) I2C host sends NACK after it gets 1-byte data, and generates a STOP bit, ending the read operation.

5.4.3. Interrupt Output

The CH9444 and CH9445 both provide 4 independent GPIOs and the interrupts generated by GPIOs can be output

through ADDR pin. The GPIO interrupt output function is enabled by setting the ADR_INT_EN bit in the system control register 0 (SYS_CTLR0) to 1. The CH9444/CH9445 will latch the current level on ADDR to control the device address in the subsequent I2C operations once this function is enabled. In this case, the level on ADDR will not affect device address, but only reflect the GPIO interrupt status. The ADR_INT_EN bit can be cleared to disable interrupt output function, and the level on ADDR pin will determine the device address.

The chip supports 4 channels for signal input and 1 channel for signal output. Set different interrupt trigger conditions for 4 GPIO pins and then configure the GPIO interrupt enable register (GPIO_INTENR) to enable the required interrupt signals.

Note: Please make sure that the ADDR pin is not shorted to VCC or GND before interrupt output is enabled. If the ADDR pin also needs to be used as address input, it is recommended to use a pull-up/pull-down resistor of dozens of KΩ or hundreds of KΩ to select the required address.

5.4.4. Switch Control

The CH9444 and CH9445 control the switches by configuring different combinations of POL/CT1/CT0, see Table-2 for details. Also, the 3 system control registers of CH9444/CH9445 provide more flexible switch control combinations. The system control register 0 (SYS_CTLR0), the system control register 1 (SYS_CTLR1) and the system control register 2 (SYS_CTLR2) can control each switch independently, with no combination limit, and can be configured reasonably as required.

If POL, CT1 and CT0 in the MUX control register (MUX_CTLR) are combined and configured to control the switches, the SEL_SW[1:0] bits in the system control register 0 (SYS_CTLR0) and all bits in the system control register 1 (SYS_CTLR1) and system control register 2 (SYS_CTLR2) need to be restored to the power-on reset value (zero).

If the system control register 0 (SYS_CTLR0), the system control register 1 (SYS_CTLR1) and the system control register 2 (SYS_CTLR2) are used to control the switches, the POL, CT1 and CT0 bits in the MUX control register (MUX_CTLR) need to be restored to the power-on reset value (zero).

6. Parameters

6.1. Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Parameter description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.4	3.8	V
VIOSBU	Voltage on input/output pins of analog switch ports #4 to #7	-0.4	VCC+0.4	V
VIOHS	Voltage on input/output pins of analog switch ports #0 to #3, #8 to #13	-0.4	VCC	V
ISW	Maximum current through analog switch	0	10	mA

6.2. Electrical Characteristics

Test conditions: TA=25℃, VCC=3.3V.

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCC	Supply voltage (VCC connects to power, GND to ground)	3.0	3.3	3.5	V
ICCS	Static current		74	200	uA
ICCSD	Low power dissipation current		2	10	uA

6.3. Electrical Characteristics of SuperSpeed Channels

Test conditions: TA=25℃, VCC=3.3V, VCM=0.3V.

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VCM	SuperSpeed signal common mode voltage	0		1.6	V
VPP	SuperSpeed signal differential voltage			1.8	V
RONS	SuperSpeed MUX (ports #0 to #3, #8 to #13) ON resistance		8	15	Ω

6.4. Electrical Characteristics of Low-speed Channel

Test conditions: TA=25℃, VCC=3.3V.

Symbol	Parameter description	Min.	Typ.	Max.	Unit
RONL	Low-speed MUX (ports #4 to #5, #6 to #7) ON resistance		4.7	8	Ω
VCMSB	Low-speed CSBU and SBU input voltage range	0		VCC	V

6.5. Timing Parameters of Channels

Test conditions: TA=25℃, VCC=3.3V, VCM=0.3V.

Symbol	Parameter description		Min.	Typ.	Max.	Unit
DILH	Differential insertion loss	0.1GHz		-0.72		dB
		2.5GHz		-0.8		dB
		4GHz		-1.8		dB
DOIH	Differential off-isolation	0.1GHz		-44		dB

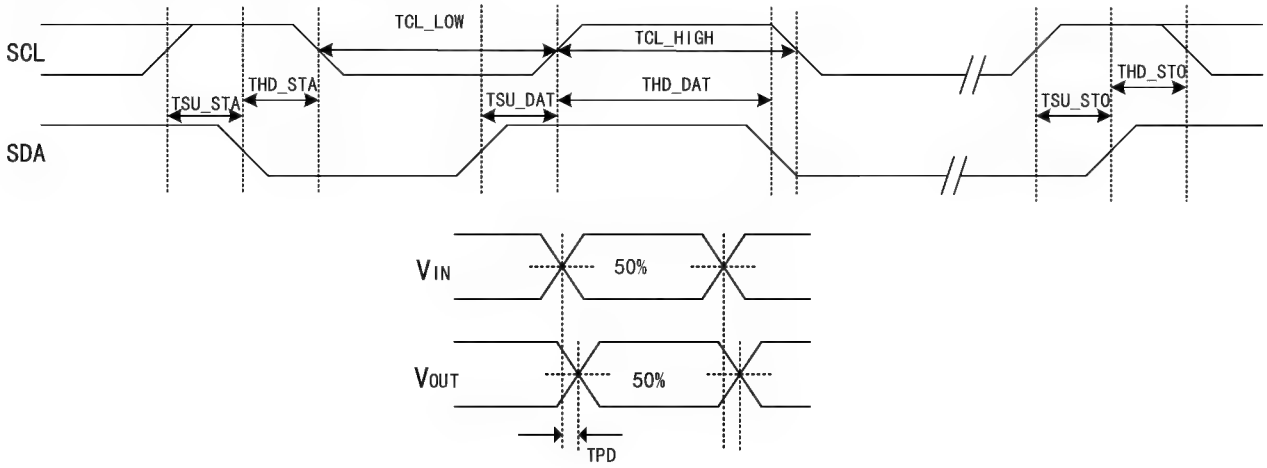
		2.5GHz		-36		dB
		4GHz		-20		dB
DRLH	Differential return loss	0.1GHz		-22		dB
		2.5GHz		-25.6		dB
		4GHz		-14		dB
NECH	Near end crosstalk	0.1GHz		-76		dB
		2.5GHz		-33		dB
		4GHz		-25		dB
BW	SuperSpeed MUX bandwidth (guaranteed by design)			6		GHz

6.6. Other Parameters

Test conditions: TA=25℃.

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VESDHS	HBM ESD voltage on high-speed channels of ports #0 to #3 and #8 to #13		3		KV
VESDLS	HBM ESD voltage on low-speed channels of ports #4 to #5 and #6 to #7		4		KV
VESDIO	HBM ESD voltage on I2C pins and GPIO pins		4		KV
VIL_I2C	Low level input voltage on SCL and SDA pins	0		0.8	V
VIH_I2C	High level input voltage on SCL and SDA pins	2.2		VCC	V
VIL_ADDR	Low level input voltage on ADDR pin	0		0.8	V
VIH_ADDR	High level input voltage on ADDR pin	2.2		VCC	V
VLVR	Low voltage reset threshold	1.7	1.9	2.2	V

6.7. Interface Timing Parameters

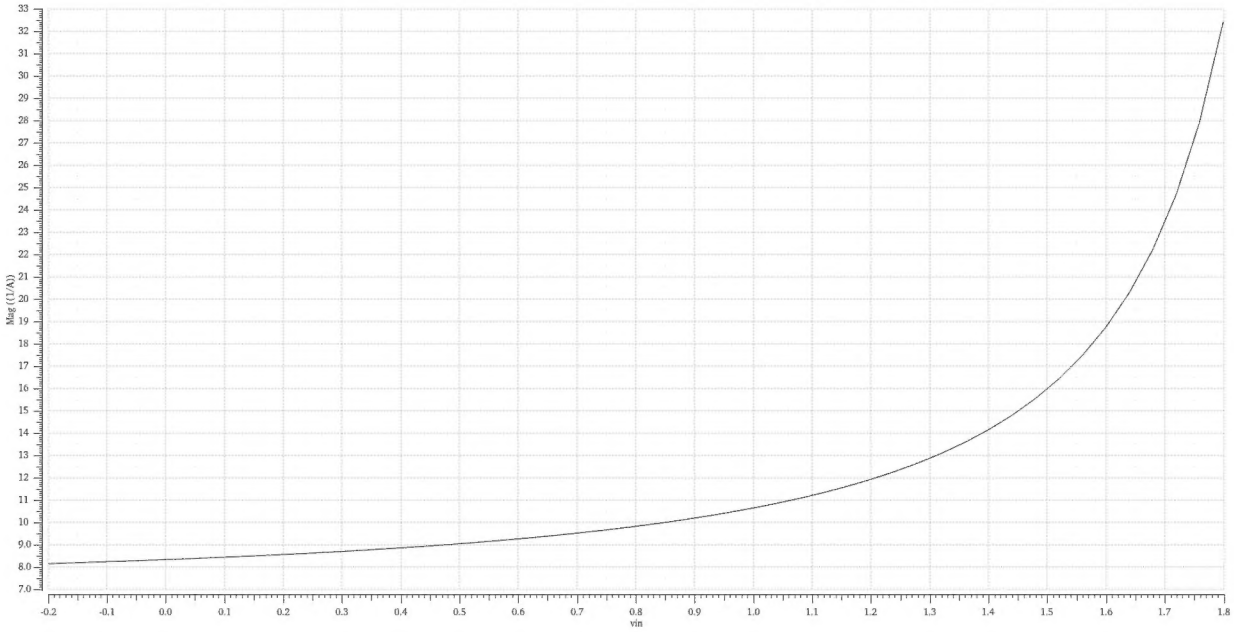


Symbol	Parameter description	Min.	Typ.	Max.	Unit
TSU_DAT	Setup time, SDA data to SCL rising edge	30			ns
THD_DAT	Hold time, SDA data to SCL rising edge	20			ns
TSU_STA	Setup time, SDA falling edge START condition	100			ns

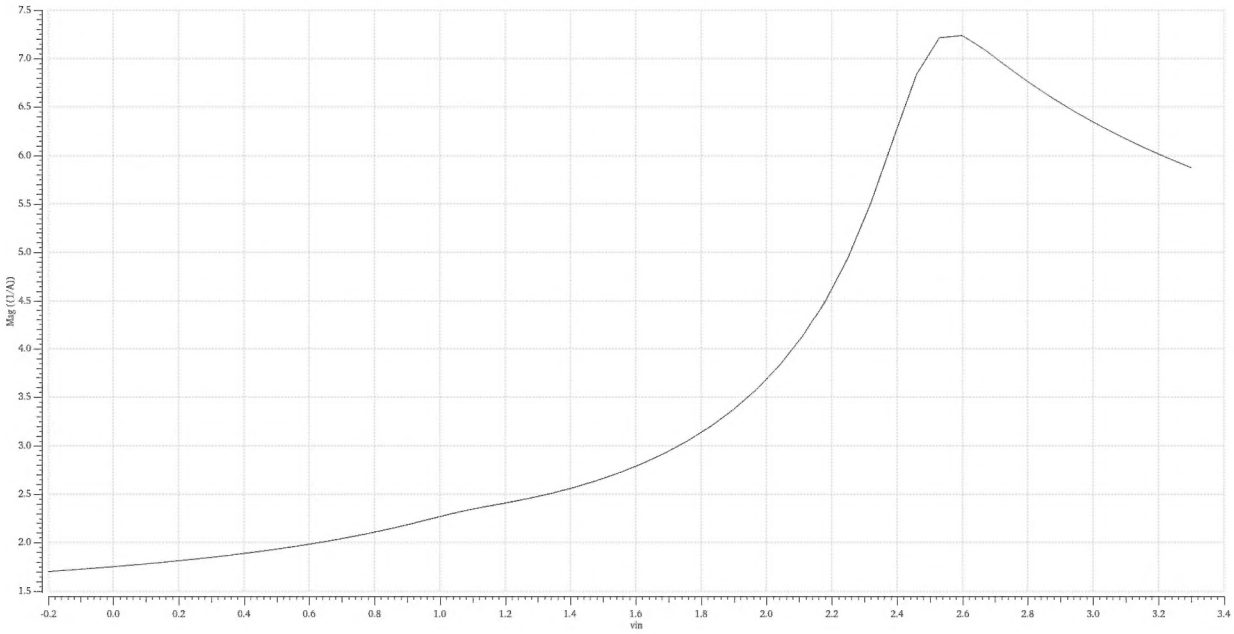
THD_STA	Hold time, SDA falling edge START condition	100			ns
TSU_STO	Setup time, SDA rising edge STOP condition	100			ns
THD_STO	Hold time, SDA rising edge STOP condition	100			ns
TCL_LOW	SCL clock signal Low width	100			ns
TCL_HIGH	SCL clock signal High width	100			ns
TONS	Mux switch ON delay		15	50	ns
TOFFS	Mux switch OFF delay		15	50	ns
TPD	Mux switch propagation delay		0.08		ns

6.8. Characteristic Diagrams

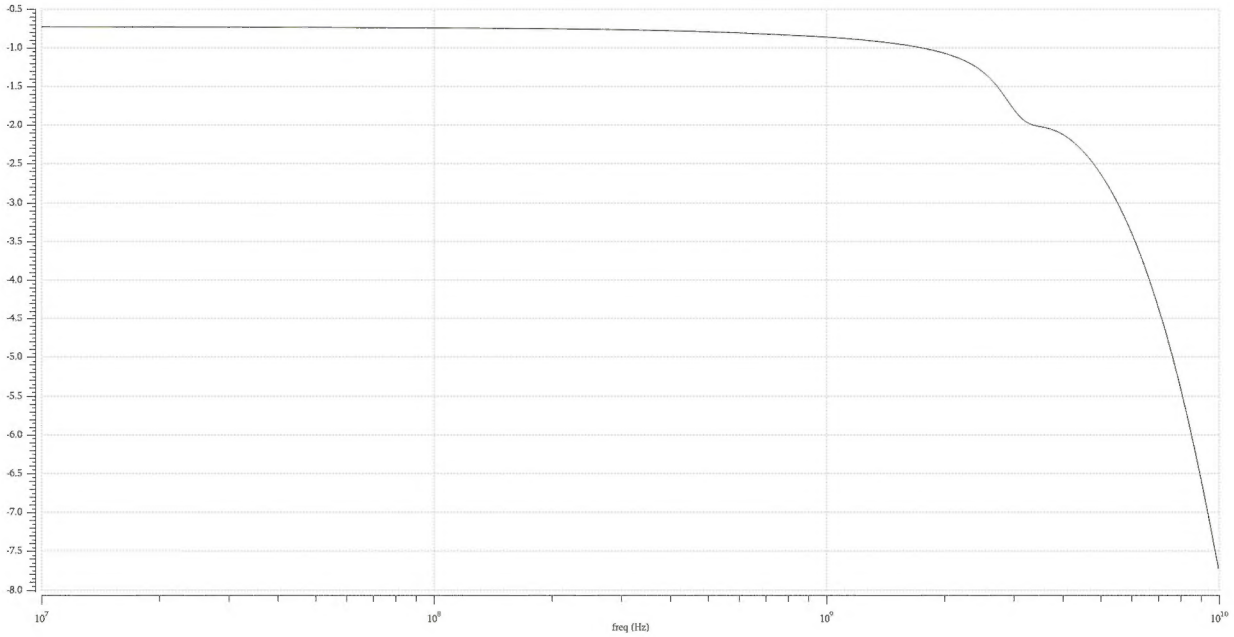
6.8.1. Correlation between MUX Ports #0 to #3 and #8 to #13 ON Resistance (RON) and Signal Voltage (VCOM)



6.8.2. Correlation between MUX Ports #4-#5 and #6-#7 ON resistance (RON) and Signal Voltage (VCOM)



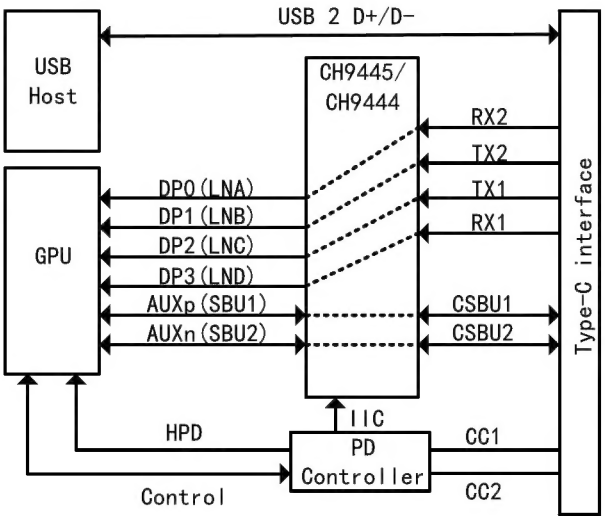
6.8.3. DILH High-frequency Characteristic of MUX Ports #0-#3 and #8-#13 ON Lanes



7. Applications

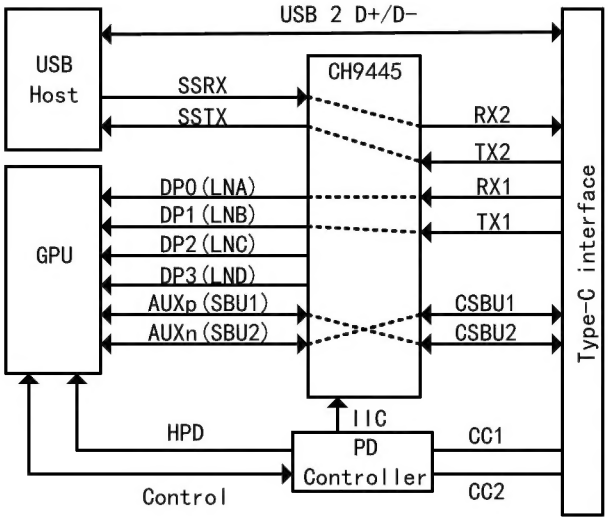
7.1. Type-C to DP Interface

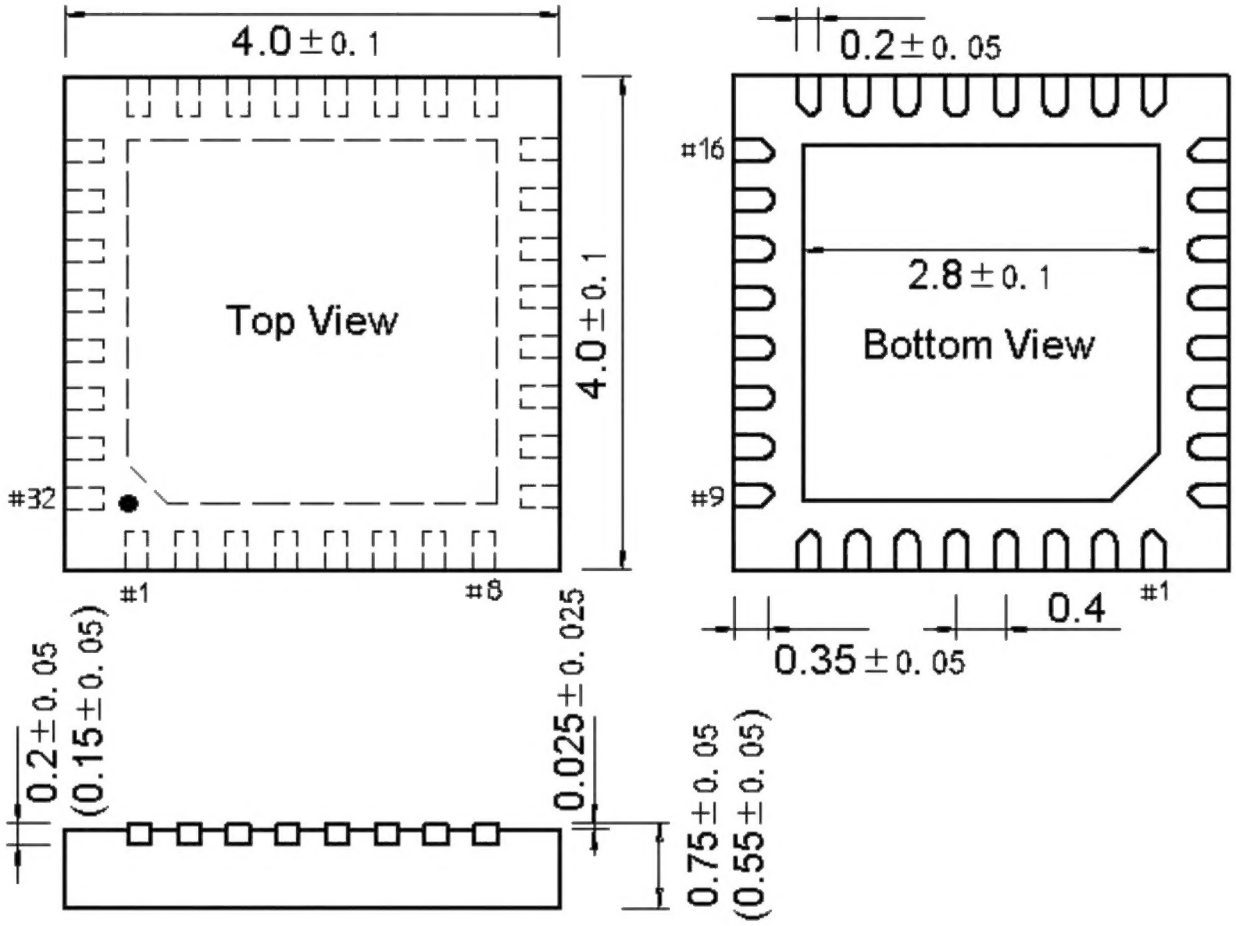
CH9444 and CH9445 can be used in the application of Type-C to DP interface. When POL/CT1/CT0=L/H/H, 4 Lane DP channel mode is selected. Four pairs of differential channels of Type-C are connected to DP interface through CH9444/CH9445, that is, ML0~ML3, PD controller MCU, such as CH32X035 or CH32L103 or CH543 chip, is only responsible for triggering DP Alt Mode and does not interfere with DP signal itself. Give full play to the complete DP output capacity of the Type-C port, on the basis of such 4 Lane trigger plus DP signal conversion, you can make a variety of Type-C to video interface lines.



7.2. Type-C to DP + USB Interface

Select 2 Lane DP+USB channel mode when POL/CT1/CT0 of the CH9445 is configured as H/L/H. The TX1 and RX1 differential channels of the Type-C interface are connected to the 2 interfaces of DP through CH9445. The RX2 and TX2 differential channels are connected to USB SuperSpeed channels through CH9445.



8. Package Information

8.1. QFN32 (4*4)